IN THE SPECIFICATION:

Please amend the second full paragraph on page 1 as follows:

As is well known, FED technology operates on the principle of cathodoluminescent phosphors being excited by cold cathode field emission electrons. ~~FIGURE~~ FIG. 1 is a simplified illustration of a representative portion of a prior art FED ~~device~~ 10. In general, the FED ~~device~~ 10 comprises a cathode assembly 6 and an anode assembly 8 separated from each other by spacers 4.

Please amend the third full paragraph on page 1 as follows:

The cathode assembly 6 is typically manufactured using conventional photolithographic processes to form successively defined features on a substrate or ~~baseplate~~ base plate 12. In general, a conductive emitter electrode structure 14 is first formed on the substrate 12. Next, a resistive layer 15 is deposited over the conductive structure 14. A pattern of spaced-apart conical cold cathode emitter tips or micropoints 18 is then formed on the substrate 12, followed by a dielectric structure 20 and a conductive or extraction grid structure 22.

Please amend the fourth full paragraph on page 1 as follows:

The substrate or ~~baseplate~~ base plate 12 is typically formed of glass. The conductive structure 14 may be formed of a metal. The micropoints 18 may be constructed of a number of materials such as, e.g., silicon or molybdenum.

Please amend the paragraph bridging pages 1 and 2 as follows:

The conductive structure 14 with the covering resistive layer 15 encircles the ~~emitters~~ emitter tips 18 of a pixel group (described below). The portions of the conductive structure 14 shown in ~~FIGURE~~ FIG. 1 are thus electrically connected and form a column line, which is part of an addressable matrix as will be described below.

Please amend the first full paragraph on page 2 as follows:

The resistive layer 15 comprising, e.g., amorphous silicon, covers the top and sides of the conductive structure 14. As shown, the outer sides of the base of each conical micropoint 18 are in contact with the resistive layer covering the conductive structure 14. The resistive layer 15 separates the conductive structure 14 from the micropoints 18 and helps prevent damage to the tips of the ~~micropoint emitters~~ micropoints 18.

Please amend the second full paragraph on page 2 as follows:

After the micropoints 18 have been formed on the base plate 12, a dielectric layer is deposited over the micropoints 18 and the resistive layer 15. The dielectric layer, which is later formed into the dielectric structure 20, may comprise silicon dioxide or other materials. Next, a conductive layer is deposited over the dielectric layer. This conductive layer, which is later formed into the extraction grid structure 22, may be made from a variety of materials including chromium, molybdenum and doped polysilicon. Then, using a photolithography/etch process, the dielectric layer and the conductive layer are etched to form the dielectric and extraction structures 20, 22, respectively, which surround, but are spaced away ~~from~~ from, the micropoints 18 as shown in ~~FIGURE~~ FIG. 1.

Please amend the third full paragraph on page 2 as follows:

The extraction grid structure 22 forms a low potential anode that is used to extract electrons from the micropoints 18. The extraction structure has a grid construction comprising multiple row lines that are orthogonal to the column lines formed by the conductive structure 14. The row and column lines are part of the addressable matrix as described below.

Please amend the paragraph bridging pages 2 and 3 as follows:

The anode assembly 8 is typically manufactured using conventional photolithography processes to form successively defined features on the lower (as shown in ~~FIGURE~~ FIG. 1) surface of the transparent substrate 24, starting with transparent conductive layer 26. The next

features usually formed are the spacers 4, which project downwardly (e.g., about 150 microns) from conductive layer 26. The black matrix grill 25 is then formed defining the pixel regions 28, in which phosphor material is deposited.

Please amend the first full paragraph on page 3 as follows:

When assembled, the anode assembly 8 is positioned a predetermined distance from the cathode assembly 6 (and from ~~micropoint emitters~~ micropoints 18) by the spacers 4.

Please amend the second full paragraph on page 3 as follows:

A power supply 30 is electrically coupled to the conductive layer 26 of the anode assembly 8 and to the conductive ~~layer~~ structure 14 (at the base of the ~~micropoint emitters~~ micropoints 18) and the conductive grid structure 22 of the cathode assembly 6. A vacuum in the space between cathode assembly 6 and anode assembly 8 facilitates travel of electrons emitted from the micropoints 18 towards the pixel regions 28 to impact the pixel regions. The emitted electrons strike the cathodoluminescent coating in the pixel regions 28, which emits light to form a video image on a display screen formed by the anode assembly 8.

Please amend the third full paragraph on page 3 as follows:

The visible display of the FED 10 is normally arranged as a matrix of pixels, one of which (single pixel 32) is shown in ~~FIGURE~~ FIG. 1. Each pixel in the display is typically associated with a group of micropoint emitters, with all emitters in a group being dedicated to controlling the brightness of their associated pixel. For example, ~~FIGURE~~ FIG. 1 shows a single pixel 32, with the pixel being associated with ~~emitters~~ emitter tips 18. For convenience of illustration, ~~FIGURE~~ FIG. 1 shows a line of four emitters as being associated with the single pixel 32. Pixel 32 could be a single pixel of a black and white display or a single red, green, or blue dot associated with a single pixel of a color display.

Please amend the paragraph bridging pages 3 and 4 as follows:

The row lines of the extraction grid structure 22 and the column lines of the emitter electrode structure 14 form an addressing matrix for selectively activating pixels. Normally, the row and column lines are arranged so that the emitters associated with one pixel can be controlled independently of all other emitters in the display and so that all emitters associated with a single pixel are controlled in unison. In operation, a row signal activates a single conductive row line within the extraction grid structure 22, while a column signal activates a conductive column line within the emitter base electrode structure 14. At the intersection of an activated column and an activated row, a grid-to-emitter voltage differential sufficient to induce field emission will exist, causing illumination of a respective pixel.

Please amend the first full paragraph on page 4 as follows:

Conventional photolithography processes are typically used to fabricate the various structures (e.g., the conductive ~~strips~~ structure 14) of the FED 10.

Please amend the second full paragraph on page 4 as follows:

It has been found in prior art FEDs that the addressing column line conductive structure 14 sometimes electrically shorts to the row line conductive structure 22. Such electrical shorting degrades the quality of the display and can even make the FED inoperative. The shorting is believed to result from manufacturing flaws in FEDs. For example, intrinsic defects in the dielectric structure 20 may effectively form conductive paths between the column addressing line and the grid. In addition, variations in the substrate and grid surfaces that cause the surfaces to be closer than intended may also cause shorting. A ~~need therefore~~ need, therefore, exists for an improved FED construction that significantly reduces the possibility of electrical shorting between column and row lines.

Please amend the first full paragraph on page 5 as follows:

The present invention is directed to an FED that has a cathode assembly containing an improved addressing column line structure. The addressing column line structure includes a conductive structure formed on a substrate. A resistive layer is formed over the conductive ~~structure,~~ structure and an insulator layer is formed partly over the resistive layer. Electrical contact between the base of the emitter tips and the addressing column line is achieved through lateral sides of the conductive structure not covered by the insulator layer. The insulator layer helps reduce the possibility of electrical shorts between the column line and the row line structure of the cathode assembly. The insulator layer on top of the addressing column line will allow the use of a thinner subsequent dielectric layer. This thinner dielectric layer, which supports the grid, will provide a lower RC time constant and help achieve better video rate operation. The thinner dielectric layer also will result in smaller grid openings above the tips. This will provide for better beam ~~spots,~~ spots and, therefore, better image resolution. The thinner dielectric layer will require less applied voltage to extract electrons from the emitter tips, resulting in lower power consumption for the FED.

Please amend the second full paragraph on page 6 as follows:

~~FIGURE~~ FIG. 1 is a ~~cross-section~~ cross-sectional view of a portion of an exemplary prior art FED;

Please amend the third full paragraph on page 6 as follows:

~~FIGURE~~ FIG. 2 is an enlarged ~~cross-section~~ cross-sectional view of a part of an FED in accordance with the ~~invention~~ invention, which illustrates a portion of an insulated addressing column line and also the lateral contact between the base of the emitter tips and the addressing column line; and

Please amend the fourth full paragraph on page 6 as follows:

~~FIGURE~~ FIG. 3 is perspective view of a portion of the FED partly broken away to illustrate the inventive addressing column line structure in greater detail.

Please amend the first full paragraph on page 7 as follows:

The present invention is directed to an improved FED, in which column addressing lines are insulated to reduce the possibility of shorting and to provide other benefits. ~~FIGURES~~ FIGS. 2 and 3 show a small portion of the cathode assembly of an FED 100 illustrating the inventive column addressing line structure 102.

Please amend the second full paragraph on page 7 as follows:

The inventive column line structure 102 (a small portion of which is shown) is preferably formed on a substrate or ~~baseplate~~ base plate 104 of the cathode assembly. The column line structure 102 comprises a conductive layer 106, a resistive layer 108, and an insulator layer 110.

Please amend the third full paragraph on page 7 as follows:

The conductive layer 106 is preferably formed like the ~~layer~~ conductive structure 14 of the FED 10 of ~~FIGURE~~ FIG. 1. It may comprise a variety of conductive materials including metals. For example, the conductive layer 106 may comprise an aluminum layer having a thickness of about 1000 Å.

Please amend the fourth full paragraph on page 7 as follows:

The resistive layer 108 is preferably similar to the resistive layer 15 in ~~FIGURE~~ FIG. 1 in that it covers the top and sides (as shown in the drawings) of the conductive layer 106. The resistive layer 108 may comprise various materials including silicon. For instance, the resistive layer 108 may be boron doped silicon having a thickness also of about 1000 Å.

Please amend the fifth full paragraph on page 7 as follows:

The insulator layer 110 has higher resistivity than the resistive layer 108. It is preferably formed to cover just the top of the resistive layer. If the insulator layer 110 also covered an entire side of the ~~resistor~~ resistive layer 108, then the insulator layer 110 might interfere with electrical communication between the conductive layer 106 and the adjacent emitter 112. Therefore, as shown in ~~FIGURES~~ FIGS. 2 and 3, insulator layer 110 preferably covers the top and not the sides of the resistive layer 108. However, in an alternative embodiment, the insulator layer 110 could also cover selected portions of the sides of the resistive layer 108.

Please amend the second full paragraph on page 8 as follows:

The insulator layer 110 is to assist in reducing shorts between the addressing column line and the row lines on the grid 116. The dielectric layer 114 is used to support the grid 116 above the ~~emitter tips~~ emitters 112. It is to be understood that the insulator layer 110 and the dielectric layer 114 may be made of the same or different material and still be within the scope of the present invention. Regardless of whether the same or different materials are used, as will be discussed below, the insulator layer 110 and the dielectric layer 114 are preferably separately formed. The insulator layer 110 reduces the possibility of shorting between the addressing column line structure and the row line structure, which as previously discussed may result from, e.g., intrinsic defects in the dielectric structure or unintended variations in spacing between the substrate and grid surfaces.

Please amend the third full paragraph on page 8 as follows:

It should be recognized that a variety of alternative materials of different thicknesses may be used for the conductive layer 106, the resistive layer 108, and the ~~insulative~~ insulator layer 110.

Please amend the fourth full paragraph on page 8 as follows:

The improved addressing line structure 102 is preferably fabricated as follows. First, the conductive layer 106 is formed on the ~~baseplate~~ base plate 104 using conventional photolithography techniques. Specifically, a layer of material from which the structure ~~106 is~~ is to be formed is first deposited on the ~~baseplate~~ base plate 104 using conventional deposition techniques. Then, using ~~conventional a~~ a conventional photolithography/etch/strip sequence, the conductive layer ~~structure~~ 106 is formed.

Please amend the first full paragraph on page 9 as follows:

Thereafter, the resistive and ~~insulative~~ insulator layers 108, 110 are formed. First, a layer of material from which the resistive layer 108 is formed is deposited over the pattern of conductive strips within the conductive layer 106. Then, a layer of material from which the insulator layer 110 is formed is deposited over the layer of resistive material. Next, using a conventional photolithography/etch/strip sequence, the resistive layer 108 and insulator layer 110 are formed on the conductive layer ~~structure~~ 106.

Please amend the second full paragraph on page 9 as follows:

To complete fabrication of the cathode assembly, the micropoint emitters 112, the dielectric ~~structure~~ layer 114, and the conductive grid ~~structure~~ 116 are then formed preferably using conventional photolithography techniques. The micropoint emitters 112 are preferably formed such that the addressing line structure 102 is disposed around (and in contact with) adjacent micropoint emitters 112 associated with a given pixel. The insulating layer deposited over the resistive layer 108, which covers the conductive ~~structure~~ layer 106, does not affect the electrical relationship between the conductive ~~structure~~ layer 106 and the adjacent emitters 112 because the sides of the addressing line structure 102 in contact with the emitters are not insulated.

Please amend the third full paragraph on page 9 as follows:

The cathode assembly formed with the inventive column addressing line structure can be assembled with a conventional anode assembly like that shown in ~~FIGURE~~ FIG. 1 to form an FED.

Please amend the paragraph bridging pages 9 and 10 as follows:

Adding the ~~insulating~~ insulator layer 110 to the addressing lines requires one additional deposition step in FED fabrication, namely the step of depositing the ~~insulating~~ insulator layer 110 on top of the ~~resistor~~ resistive layer 108. However, no extra photolithography sequences are required for forming the ~~insulating structure~~ insulator layer 110 because the insulator and ~~resistor~~ resistive layers 110, 108 are etched from a single mask pattern. This is possible because when viewed from the top, in the preferred embodiment of the addressing ~~line,~~ line (as shown in ~~FIGURE 2)~~ FIG. 2), the outer edges of the ~~insulating structure~~ insulator layer 110 and the underlying resistive layer ~~structure~~ 108 are substantially aligned, i.e., the insulator ~~structure~~ layer 110 substantially exactly overlies the ~~resistor~~ resistive layer 108. Therefore, no extra photolithography (or masking) steps are needed, which are well known to be costly, complex and time consuming.

Please amend the first full paragraph on page 10 as follows:

Many variations of the above-described preferred embodiments are possible. For example, one alternative embodiment might include more layers than the above-described combination of an insulator layer 110 and a resistive layer 108. For example, multiple resistive ~~layers,~~ layers could be layered on top of one another to form a suitably high series resistance.

Please amend the third full paragraph on page 10 as follows:

The insulated column line structure also provides other advantages. For instance, addition of the ~~insulative~~ insulator layer 110 increases the distance between the conductive layer 106 and the grid ~~structure~~ 116. This improves the ~~FED'S~~ FEDs' refresh rate by decreasing

the associated RC constant. ~~'R'~~ "R" is the resistance of the conductive lines (both grid and ~~column),~~ column) and ~~'C'~~ "C" is the capacitance between a column line and the grid layer. C is proportional to A/d (where ~~'A'~~ "A" is a ~~cross sectional~~ cross-sectional area and ~~'d'~~ "d" is the distance between the plates). By increasing d, C is reduced, which thereby reduces the RC constant. The reduced RC time constant will assist in achieving a better video rate operation of the display.